A CURRENT SWEEP METHOD FOR ASSESSING THE MIXED-MODE DAMAGE SPECTRUM OF SIGE HBTS

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A CURRENT SWEEP METHOD FOR ASSESSING THE MIXED-MODE DAMAGE SPECTRUM OF SIGE HBTS

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[To my dear mother and father]

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I wish to thank my God and my Savior, Lord Jesus Christ, for guiding me in this life and instilling in me the passion and desire for knowledge. In addition, God blessed me with a great advisor, Dr. Cressler, who remains a relentless guiding force for my research. I would like to especially thank my mother and father, without whose guidance and support I would not be here.

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SUMMARY

In this work a new “current-sweep” stress methodology for quantitatively assessing the mixed-mode reliability (simultaneous application of high current and high voltage) of advanced SiGe HBTs is presented. This stress methodology allows one to quickly obtain the complete “damage spectrum” of a given device from a particular technology platform, enabling better understanding of the complex voltage, current, and temperature interdependence associated with electrical stress and burn-in of advanced transistors. We consistently observed three distinct regions of mixed-mode damage in SiGe HBTs, and find that hot carrier induced damage can be introduced into SiGe HBTs under surprisingly modest mixed-mode stress conditions. For more aggressively scaled silicon-germanium technology generations, a larger percentage of hot carriers generated in the collector-base junction are able to travel to and hence damage the EB spacer, leading to enhanced forward-mode base current leakage under stress. A new self-heating induced mixed-mode annealing effect was observed for the first time under fairly high voltage and current stress conditions, and a new damage mechanism was observed under very high voltage and current conditions. Finally, as an example of the utility of our stress methodology, we quantified the composite mixed-mode damage spectrum of a commercial third-generation (200 GHz) generation SiGe HBT. It is found that if devices are stressed with either voltage or current alone during burn-in, they can easily withstand extreme over-stress conditions. Unfortunately, devices were easily damaged when stressed with a combination of stress voltage and current, and this has significant

implications for the device and circuit lifetime prediction under realistic mixed-signal operating conditions.

CHAPTER 1

INTRODUCTION

As SiGe HBTs continue to scale and improve in their performance capabilities, potential reliability challenges begin to emerge. Peak cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) have rapidly increased with each succeeding SiGe hetero-junction bipolar generation, from 50 GHz (1st generation) to 100 GHz (2nd generation), to 200 GHz (3rd generation), and early prototypes of 300 GHz technologies now exist. These impressive scaling achievements have been made possible by lateral scaling to minimize parasitics, thermal cycle reduction, incorporation of carbon doping to suppress boron out-diffusion, germanium profile engineering, and careful collector profile engineering needed to delay the onset of base push-out so that robust operation at high current density can be achieved. Scaling-mandated increases in operating current density, the higher electrical fields due to higher doping levels, and potentially worsening self-heating effects due to increasingly higher operating current density, all combine to present a formidable challenge to device and circuit reliability. Understanding the subtleties of these phenomena, and importantly how they interplay with and against one another, makes reliability physics a complex topic in SiGe HBT.

In the past, bipolar technologies suffer from two reliability issues. The first is high forward current density damage (voltages used in the base and collector are very low, thus this is not a hot carrier phenomenon), due to the electromigration of the emitter contact to the polysilicon emitter. This leads to an increase in the overall emitter doping, resulting in unusual characteristics in current gain. The second is reverse-EB stress, when the base voltage is driven lower than the emitter voltage (which is often the case with BiCMOS digital logics), causing hot carriers to create leakage base current. Due to the

base resistance, the leakage current will produce an undesirable voltage offset at the input of the circuit.

Observing the various technology trends in rough numbers may be able to shed light on an emerging reliability issue in SiGe HBTs, different than reverse-EB and high-current stress. 1st generation devices have a peak f_T of 50 GHz at $j_c \sim 1$ mA/um^2 and has BV_{ceo} of 3.3 V; 2nd generation devices have peak f_T of 100 GHz at $j_c \sim 7$ mA/um^2 and has BV_{ceo} of 2.5 V; 3rd generation devices have peak f_T of 200 GHz at $j_c \sim 10$ mA/um^2 with $BV_{ceo} = 1.8$ V. f_T has been doubling for each generation of SiGe technology; however current densities needed to reach the peak f_T have increased nearly 10x, and breakdown voltages have also fallen by nearly 2x.

This has strong implications on the circuit's performance and reliability: attenuation in the atmosphere is more severe at higher frequencies, thus more output power would be needed for higher frequencies of operation. With the increasing current densities, it could be argued that higher generation devices can output more power, even due to the lower breakdown voltage: one could simply drive very large currents to compensate for the loss in voltage. However, this implies very large devices (traditionally done by chaining many devices in parallel), which maybe impractical due to 1) frequency performance degradation, 2) increased loss in the metals and vias, 3) yield issues due to the large sizes, 4) degradation in power efficiencies, 5) self-heating due to the high current densities, and most important of all 6) difficulties involved in power matching for optimal load impedance. Due to these constraints mainly brought on by progressive scaling with each succeeding generation, many circuit designers have attempted to "cheat" the system by operating devices above BV_{ceo}. Needless to say, this presents a new reliability issue not addressed in high current density stress and reverse-EB stress.

By stressing devices in these high-current and high-voltage conditions, a new reliability damage mechanism was recently observed in SiGe HBTs, and is called "mixed-mode" electrical stress [1]. Its damage characteristics indeed differ from those of

reverse-EB stress or high forward current density stress, which have traditionally been used in burn-in of high-speed bipolar transistors. In mixed-mode stress, when devices are exposed to a combination of high collector voltage and high emitter current, *both* forward- and reverse-mode base current damage results. Figure 1 illustrates this phenomenon. Forward-mode base current (holes) travels close to the emitter-base (EB) spacer, whereas reverse-mode base current travels close to the shallow trench isolation (STI) [2], and thus observing leakage in both modes of operation indicates that hot carriers are propagating in different directions, producing interface traps at both the EB-spacer and STI interfaces.

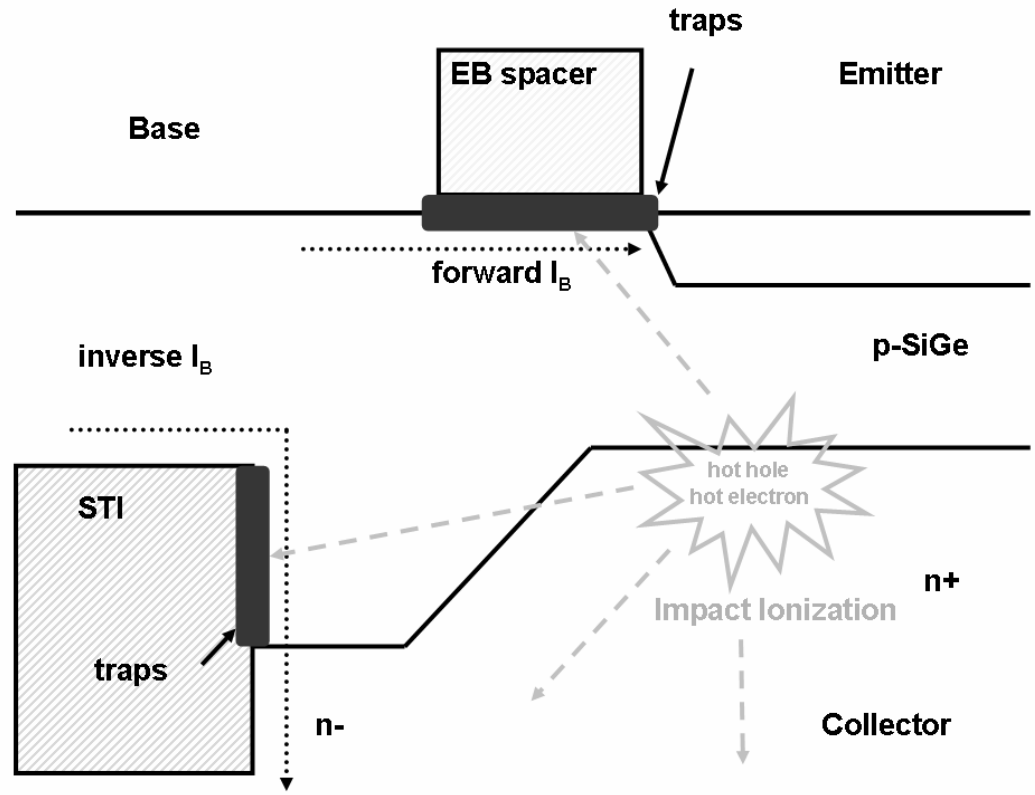

Figure 1. Cross-section of a SiGe HBT, which shows the paths of forward-mode and reverse-mode base current. Forward base-current samples the interface traps at the EB spacer, and reverse base current samples interface traps at the STI.

Efficient and accurate stress techniques are essential for device reliability analysis and meaningful device lifetime projections. This is especially relevant for mixed-mode stress since the damage is known to depend on the stress current, voltage, and ambient temperature [3]. Given the wide variety of relevant operating conditions a transistor can experience in mixed-signal circuit operation, as well as the large variety of SiGe technologies available, and the many different device geometries used, combine to make the size of the mixed-mode stress matrix quite a daunting challenge. In order to better understand the damage processes engaged, we employ a very large range of stress conditions in order to observe the boundaries of the various damage mechanisms. The ranges of stress current density ($J_{E,str}$) and voltage ($V_{CB,str}$) used are shown in Figure 2, and compared with previous work. Reliability results from four SiGe technologies are reported. During mixed-mode stress, collector-base voltage was varied from 0V to 9V, and emitter current density was varied from 1 nA/μm^2 to 100 mA/μm^2. Most of the reported data were measured at room temperature. However, some low (100 K) and high (400 K) temperature stress experiments were also included to better understand the underlying damage physics.

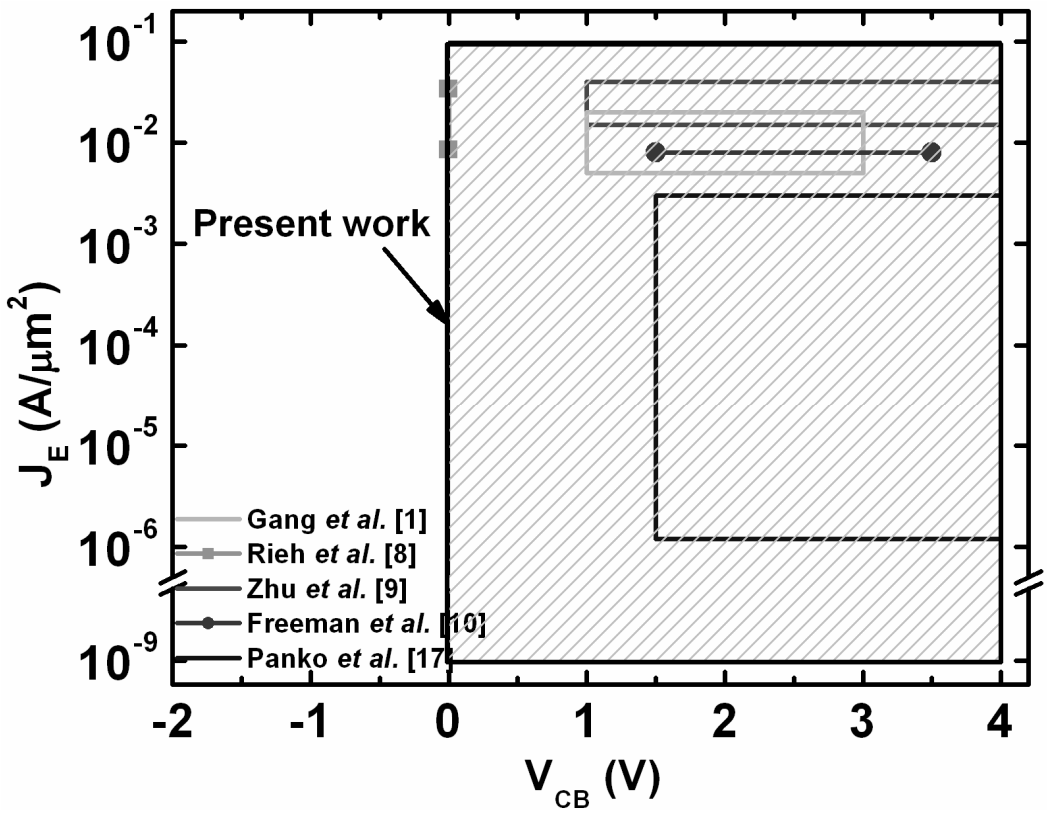

Figure 2. Stress conditions used in this work compared with other studies. A large range of stress conditions were used to understand which damage mechanisms dominate at what stress conditions.

We first introduce a new stress measurement methodology called mixed-mode "current-sweep". Then, applying this methodology to various SiGe HBTs three different damage regions are identified: 1) low-current mixed-mode stress, 2) mixed-mode annealing, and 3) high-current mixed-mode stress. The first region is associated with hot carriers created in the collector-base junction. This is the main focus of the paper, because it is most critical to circuit reliability. This damage mechanism increases dramatically with profile scaling, posing an increasingly critical reliability issue as SiGe technology evolves. The second damage region, mixed-mode annealing, represents a self-heating induced process that can be seen under particular stress conditions, and it is shown to have significant implications for accurately assessing inferred reliability lifetimes. The third damage region (high-current mixed-mode stress) occurs under extremely aggressive mixed-mode stress conditions, and has a very different damage signature than for traditional hot carrier stress. Finally, the overall damage spectrum of third-generation SiGe HBTs is presented as an example of applying our stress methodology and illustrates the context of the three mixed-mode damage regions.

CHAPTER 2

DEVICE TECHNOLOGIES

The devices investigated in this work represent three generations of commercially-available SiGe HBTs. SiGe HBT A is a third-generation 130 nm SiGe technology, with a peak f_T=200 GHz and BV_{CEO}=1.7 V [4]; SiGe HBT B is a second-generation, 180 nm SiGe technology, with peak f_T=120 GHz and BV_{CEO}=2.5 V [5]; SiGe HBT C is a first-generation, 0.5 μm SiGe technology, peak f_T=50 GHz and BV_{CEO}=3.3 V [6]; and SiGe HBT D is a third-generation SiGe technology with 130 nm lithography, and has peak f_T = 200 GHz and BV_{CEO} = 2.0 V [7]. The avalanche multiplication factors for SiGe HBT A, B and C are shown in Figure 3. At a fixed voltage, the M-1 of the 2nd and 3rd generation SiGe HBT are comparable and about ten times higher than M-1 for the first generation device due to the higher collector doping.

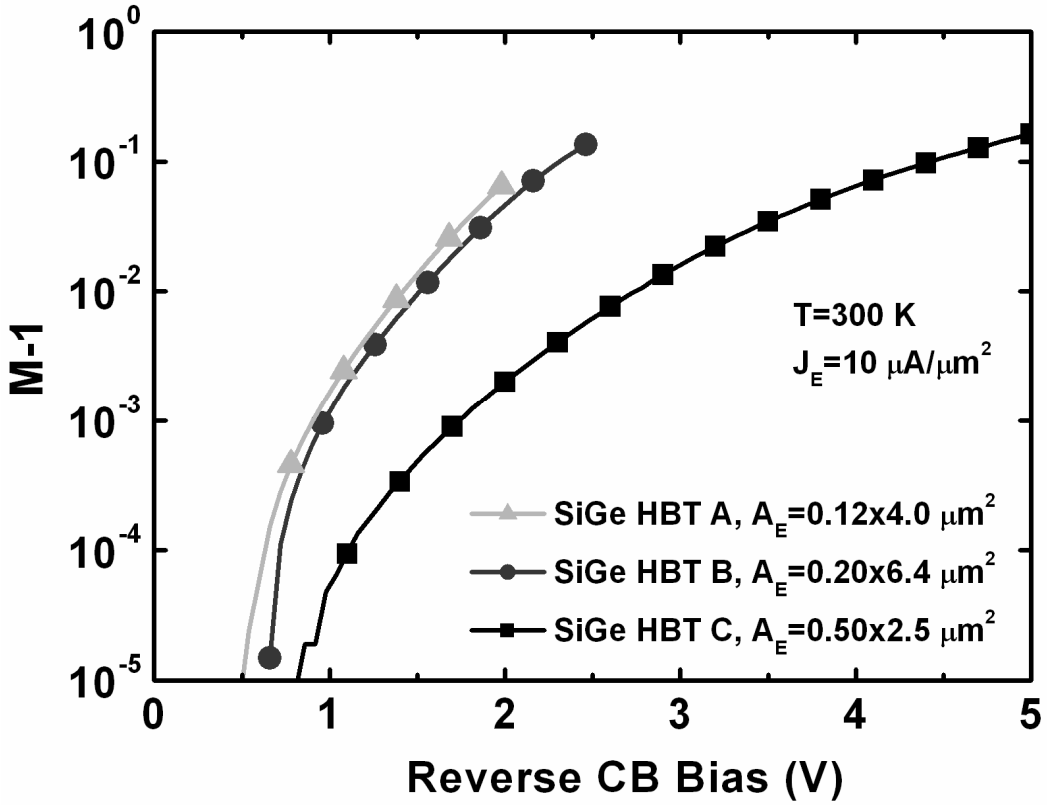

Figure 3. Comparison of the avalanche multiplication factor of SiGe HBT A (3rd gen.), B (2nd gen.), and C (1st gen.).

The thermal resistances of the transistors were measured using the method described in [8]. The values are shown in Figure 4, which is similar to those reported in [9]. It could be seen that the thermal resistance is independent of the emitter width, but is instead dependent on emitter area, and the structural changes necessitated by scaling have not had a significant impact on R_{th}. For identical emitter area and stress condition, data in Figure 4 indicates that the thermal resistances remain approximately constant with technology scaling, and thus we expect the thermal resistance for future technology nodes do not *necessarily* suffer from enhanced self-heating for fixed operating conditions. Comparing the effects self-heating across technologies has some subtleties. If comparing at the same RF frequency of operation (say, f = 2GHz and comparing SiGe HBT A and SiGe HBT C), then certainly self-heating would be less in higher generations, since higher generation devices can achieve much higher gain and can the high $J_{C,peakfT}$ allows more RF output power. Since self-heating is the product of total dissipated power and thermal resistance, for the same dissipated power higher technology devices should show the same amount of self-heating. However, this is not a realistic comparison since higher generation technologies are too expensive to be competing with lower technologies. If self-heating is compared at their respective peak f_t (or fixed ratio of it), then higher generation technologies would be worse.

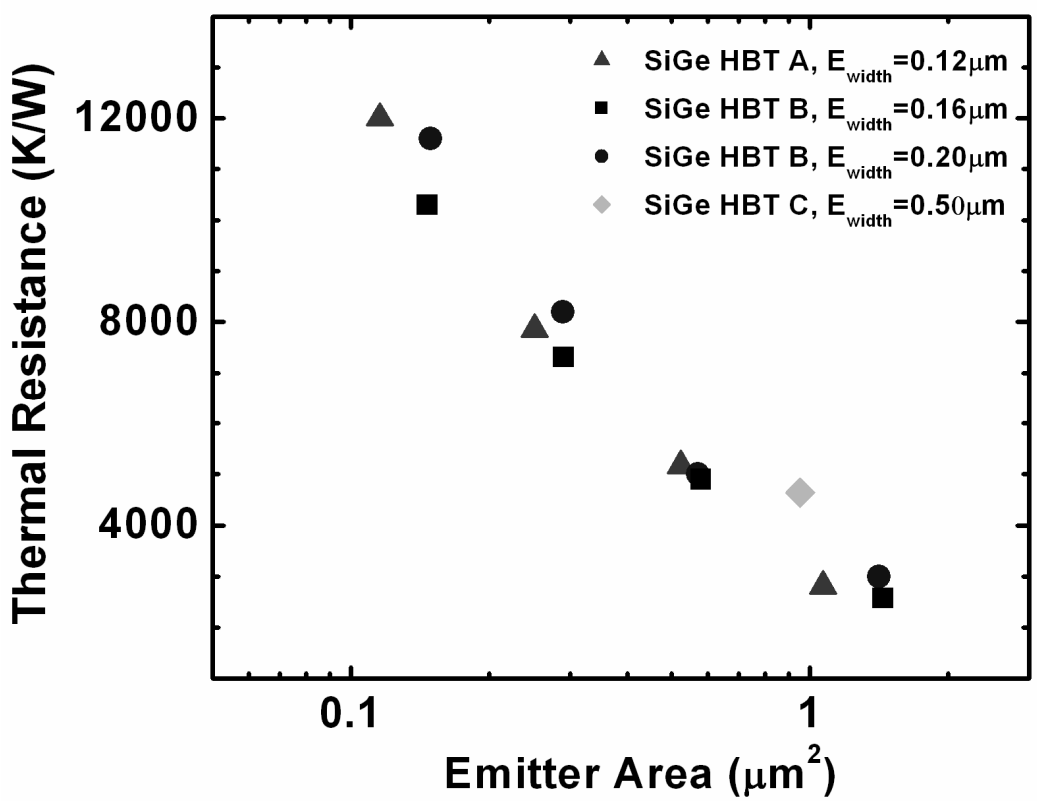

Figure 4. Thermal resistance of SiGe HBT A and B. Emitter width of 0.12 μm was used for SiGe HBT A; 0.16 μm and 0.20 μm were used for SiGe HBT B.

CHAPTER 3

EXPERIMENT

All *dc* measurements reported here were performed using an Agilent 4155C Parameter Analyzer. For each measurement, multiple devices were measured to ensure consistency of trends. For the mixed-mode stress measurement described in [10], transistors were biased in common base mode, and stressed with a fixed emitter current and collector voltage. Stress was interrupted periodically to measure the Gummel characteristics. Essentially, the stress methodology described in [10] probes the time evolutions of the damage mechanism. The current-sweep methodology presented here is similar to [10], except that the stress bias (current or voltage) were successively increased while using a fixed stress time interval. In effect, the current-sweep measurements probe the impact of the stress bias conditions on the resultant damage.

A typical current-sweep experiment occurs as follows. First, the pre-stress forward and inverse Gummel characteristics were measured. Next, the device was stressed at a fixed $V_{CB,str}$ (e.g., 3.0 V) and at an emitter current density ($J_{E,str}$) of 1.0 nA/μm^2, for a certain stress time interval (t_{str}). Gummel characteristics were measured after the applied stress, and then the device was stressed again at the same fixed $V_{CB,str}$ and t_{str}, but with larger $J_{E,str}$. This process of iterative stress, post-stress measurement, and then incrementally increased $J_{E,str}$ was continued until the device suffers complete failure, in which the devices were either short- or open-circuited. Usually this failure happened at extremely high $J_{E,str}$ (~100 mA/μm^2). In order to ensure measurement efficiency, $J_{E,str}$ is increased exponentially until it reaches ~1 mA/μm^2, and then linearly increased to ~100 mA/μm^2. Current sweeps are usually plotted as normalized ΔI_B at V_{BE}=0.6 V versus $J_{E,str}$, and the stress intervals used were typically 10 s. We would like to make clear that the normalized ΔI_B plotted represents the accumulated mixed-mode damage of the device.

Variations of current-sweep conditions spanning the relevant reliability matrix can thus be readily performed. Simultaneously increasing $V_{CB,str}$ and $J_{E,str}$ obtains the entire damage spectrum ($V_{CB,str}$ from 0 V to 10 V, and $J_{E,str}$ from 1 nA to 100 mA/μm^2) with only about 8 devices and 2 hours of stress time.

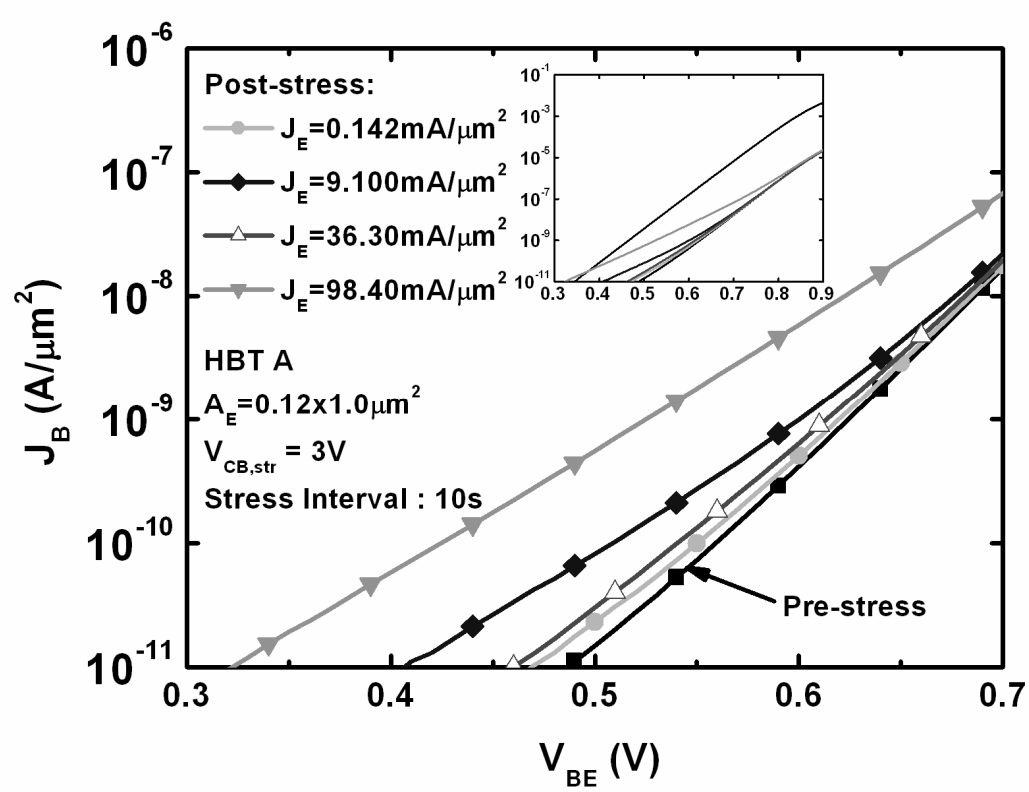

Figure 5. Gummels during the current-sweep stress measurement. The excess base current exhibits an ideality factor close to 2, indicating the classical SRH recombination through interface traps.

Typical pre- and post-stress Gummels measured during a current-sweep measurement of SiGe HBT A are shown in Figure 5. Observe that at $J_{E,str}$=0.142 mA/μm^2 and $V_{CB,str}$=3 V, I_B began to show a slight deviation from its pre-stress I_B. Given the high $V_{CB,str}$ applied, SiGe HBT A was expected to show damage under these conditions [11] due to the large number of hot carriers, yielding increased damage. When the stress current density exceeded $J_{C,peak\ fT}$, the peak electric field decreased due to base pushout [12], and thus ΔI_B was expected to saturate at these current densities. Contrary to this naïve assumption, however, the excess base current actually decreased after $J_{E,str}$ =36.30 mA/μm^2. As $J_{E,str}$ was increased even further (to 98.4 mA/μm^2), ΔI_B increased again, to the point where the device became non-functional (not shown). The base leakage current is shown more clearly in Figure 6, where normalized ΔI_B was plotted versus $J_{E,str}$. The current-sweep of two other devices stressed with t_{str} = 50 s, and t_{str} = 250 s at the same bias conditions are also included. Note that the normalized ΔI_B followed a consistent trend that can be characterized by a "hump" shape, followed by a sharp rise. This behavior could be investigated as three separate damage regions. The rising portion of the "hump" (40 μA/μm^2<$J_{E,str}$<9 mA/μm^2) constitutes "low-current mixed-mode damage" (or Region I). The falling portion of the hump (10 mA/μm^2< $J_{E,str}$<40 mA/μm^2) represents "mixed-mode annealing" (or Region II), and finally, the sharp-rise region ($J_{E,str}$> 40 mA/μm^2) represents "high-current mixed-mode damage" (Region III). It is important to note that the boundaries of these three regions vary with $V_{CB,str}$, temperature and geometry, and the physics behind these dependences will be examined in detail in the following section.

Figure 7 compares current-sweeps of different SiGe HBT technologies, all measured with the same $V_{CB,str}$ and t_{str}. Region I and II (the "hump" region) is not observed for the first generation device, but it could be observed in the second-generation device, and the hump shape is even more noticeable in the two 3rd generation devices,

clearly demonstrating the role of scaling. However, it is interesting to observe that whereas Region I and II become more apparent with scaling, Region III appears to have no clear trend with scaling.

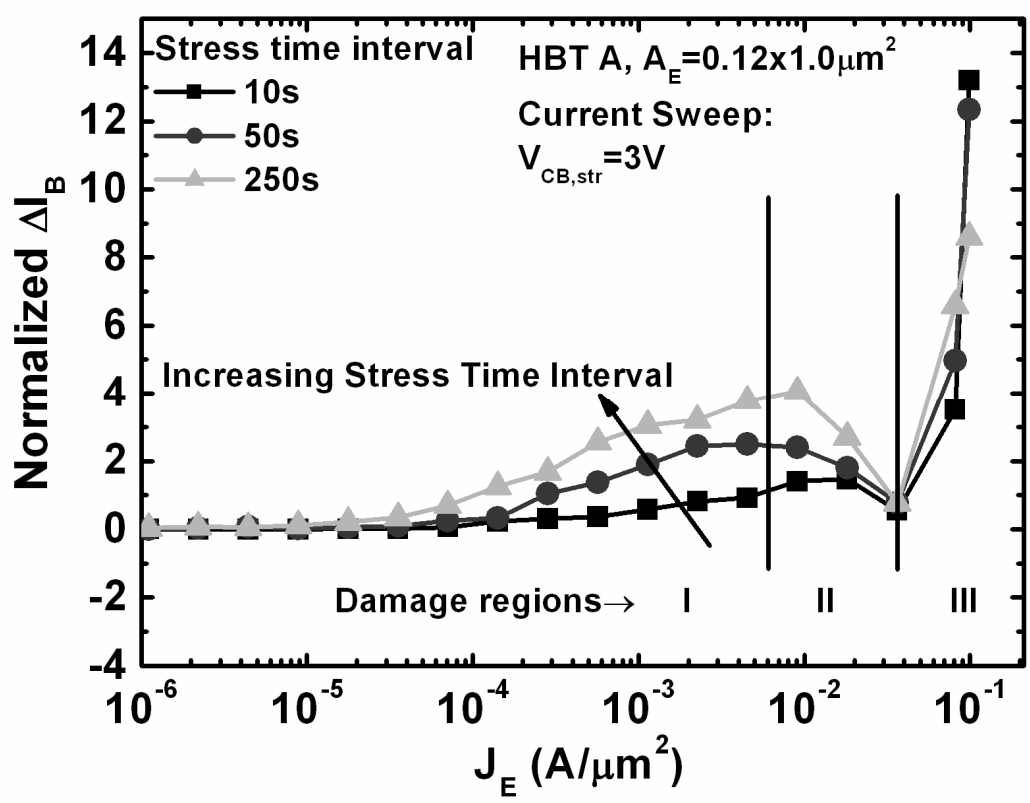

Figure 6. Current-sweeps of SiGe HBT A, with different stress time intervals. The hump shape becomes more apparent with longer stress times. Normalized ΔI_B was defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

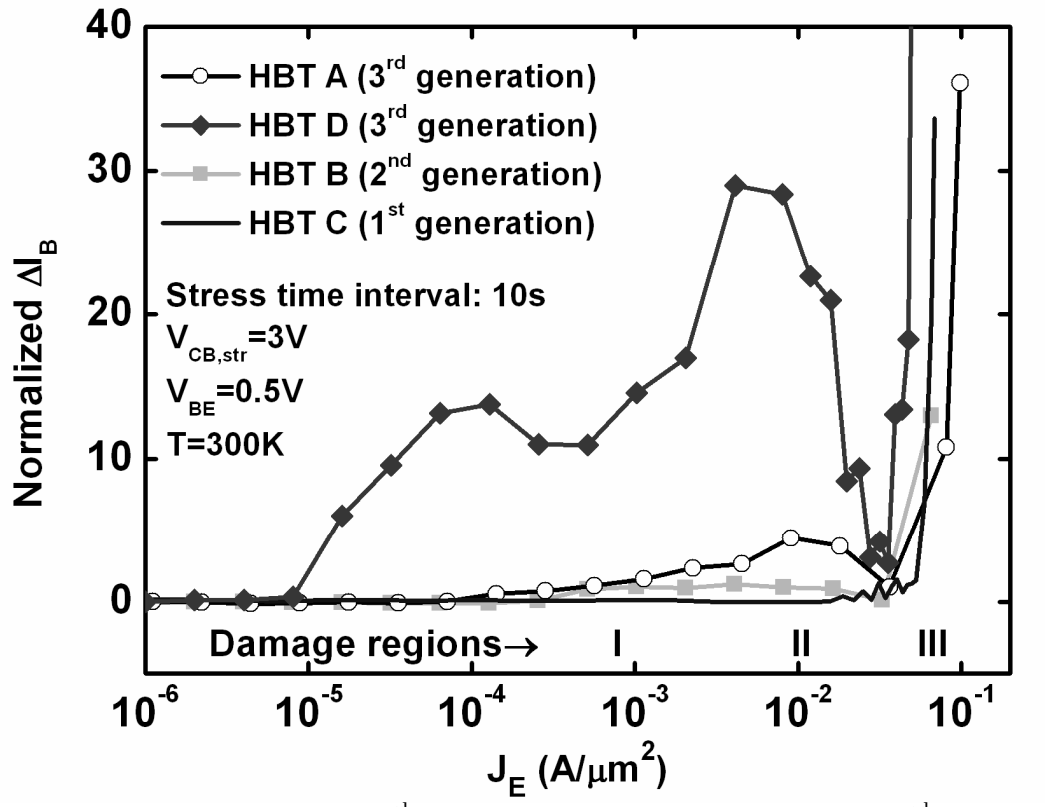

Figure 7. Current-sweeps of two 3rd generation SiGe HBTs (200 GHz), a 2nd generation (100 GHz), and a 1st generation (50 GHz) HBT. Normalized ΔI_B is defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

CHAPTER 4

REGION I: LOW-CURRENT MIXED-MODE DAMAGE

Figure 8 shows current-sweep results for HBT A, with $V_{CB,str}$ = 3 V and $V_{CB,str}$ = 4 V. Observe that the damage response was significantly increased with higher $V_{CB,str}$. The time dependence of the low current damage in HBT A ($J_{E,str}$ and $V_{CB,str}$) is shown in Figure 9 to be proportional to $\sim t^{0.5}$. The excess I_B exhibited an ideality factor near 1.8, which indicates classical space charge region SRH recombination (a more detailed derivation of the ideality factors and its implications are shown in Appendix A). In addition, inverse-mode Gummel characteristics showed a similar degraded base current, indicating hot carriers in the CB junction damage both the STI and EB spacer. All of these characteristics were similar to previous work reported in [10, 11, 13], which concluded that the stress-induced damage was the result of hot carriers under high reverse bias in the collector-base junction traveling towards both the EB spacer and STI. Some of these hot carriers will subsequently create a silicon 'dangling' bond, producing traps near the Si/SiO_2 interface. Higher $V_{CB,str}$ will generate more energetic carriers, and thus more damage was produced.

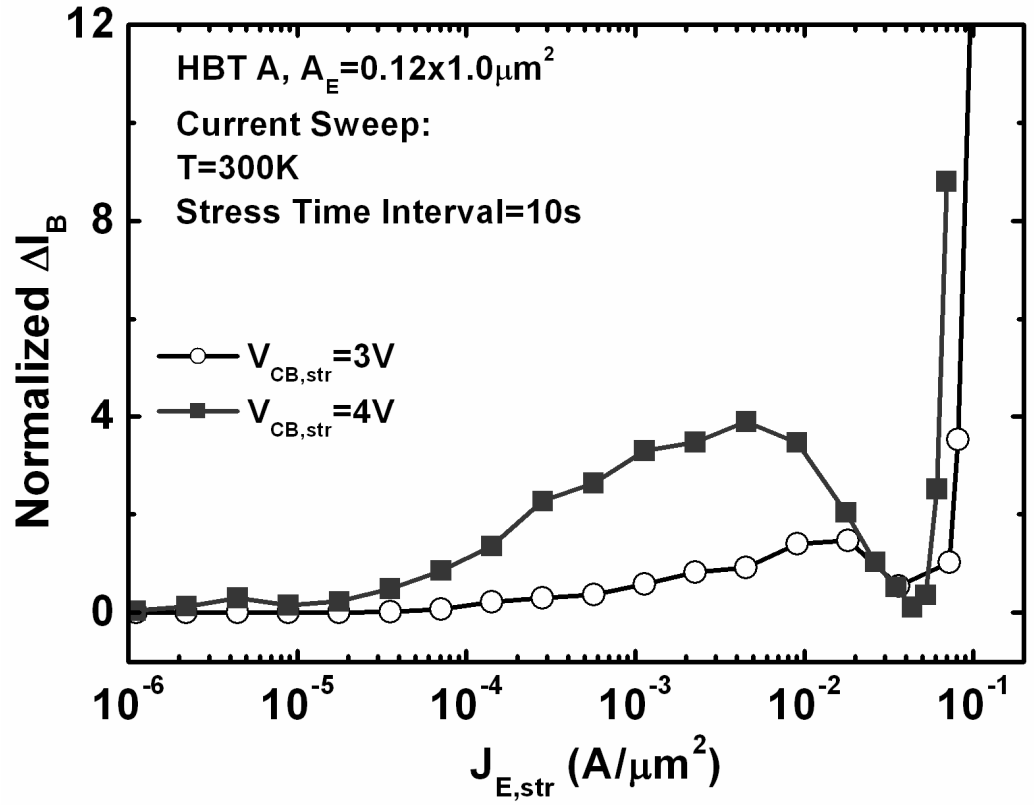

Figure 8. Current-sweeps of HBT A, using different values for $V_{CB,str}$. The hump shape dramatically increases while the high-current stress shifts slightly to the left.

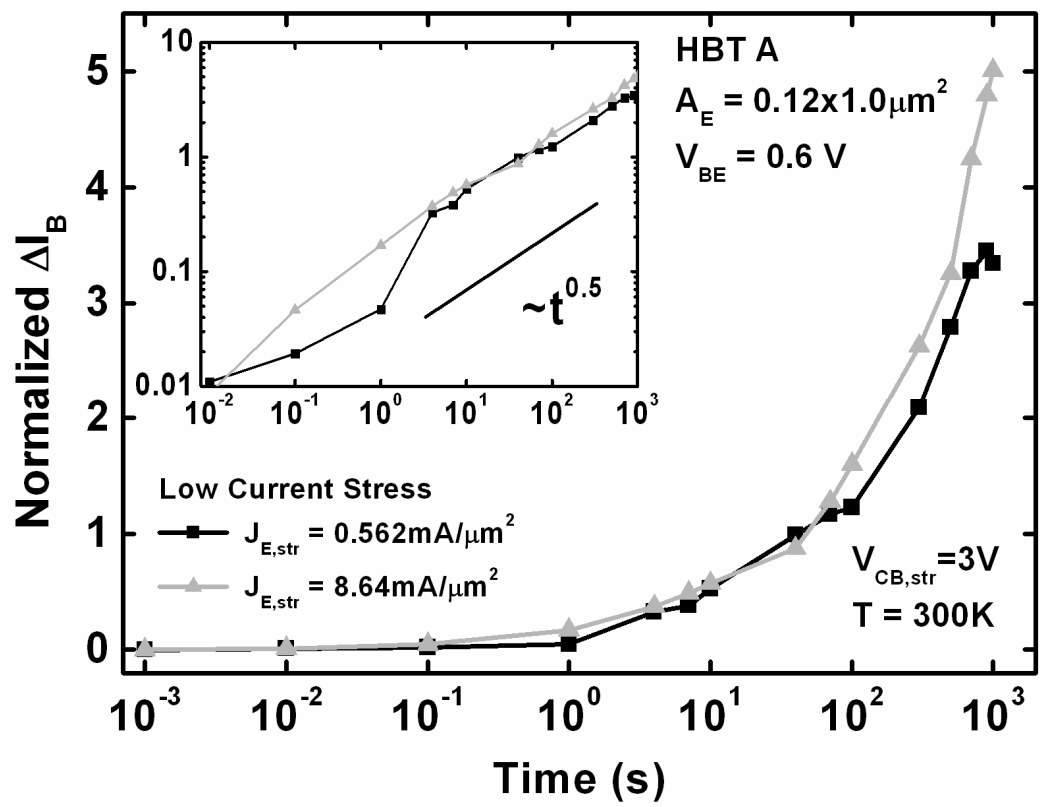

Figure 9. Low-current stress of HBT A's. Low-current stress is observed to have consistent $t^{0.5}$ dependence. Normalized ΔI_B was defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

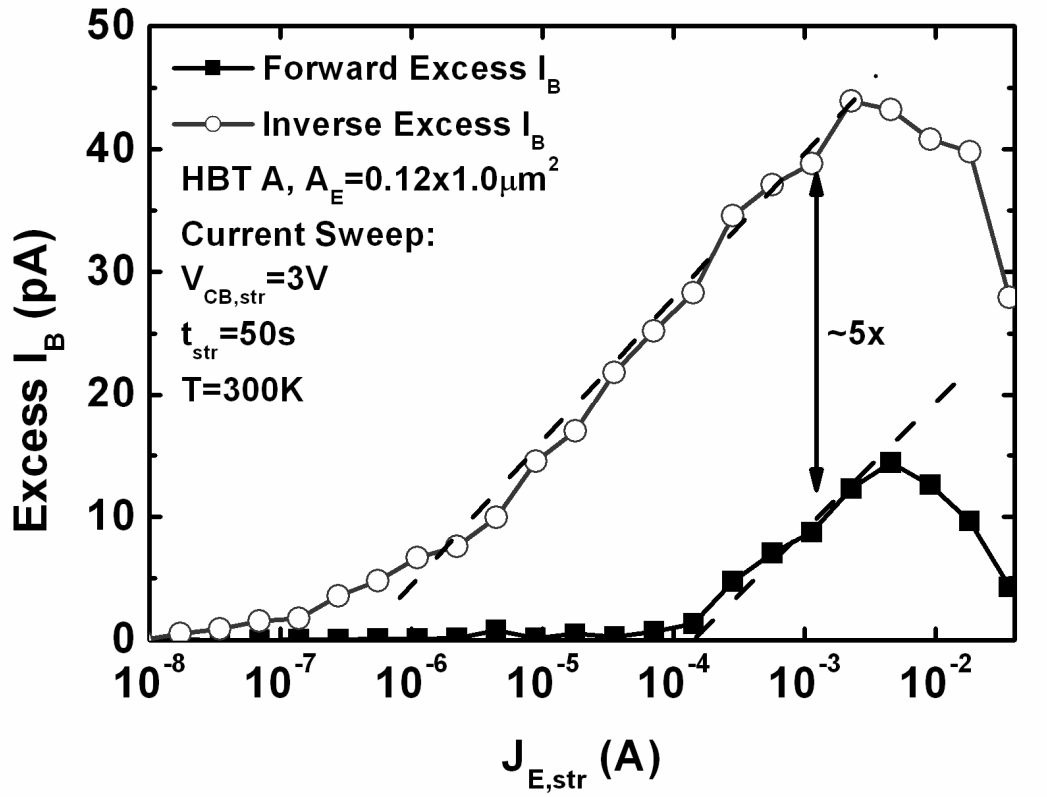

Figure 10. Forward-mode and reverse-mode excess base current, as a function of $J_{E,str}$. Reverse-mode base current was approximately five times the forward-mode base current.

Using current-sweep stress, we can gain additional insight into the damage mechanisms by comparing the excess forward and reverse base currents ($\Delta I_{B,for}$ and $\Delta I_{B,rev}$), as shown in Figure 10. Note that this comparison is valid only when ideality factors (n) of the two leakage currents are close to 2, indicating an absence of significant trapped charge. The $\Delta I_{B,rev}$ becomes apparent at much lower $J_{E,str}$ than $\Delta I_{B,for}$. At a fixed $J_{E,str}$, $\Delta I_{B,rev}$ was about five times that of $\Delta I_{B,for}$. This is expected, because the STI is located much closer to the CB junction than the EB spacer, and therefore much more prone to hot carrier damage. In order to simplify the comparison of $\Delta I_{B,for}$ and $\Delta I_{B,rev}$, oxide charge is assumed to be negligible. Then ΔI_B resulting from hot carrier stress in a linearly graded *pn* junction can thus be defined as [14]

$$\Delta I_B = \frac{1}{2} q n_i P_E \sigma v_{th} N_T \exp\left(q \frac{V_{BE}}{2kT} \right) \Delta L \tag{1}$$

where P_E is the perimeter, σ is the capture cross-section, v_{th} is the thermal carrier velocity, N_T is the trap density, and ΔL is defined as the effective width over which recombination occurs. If V_{th}, σ, ΔL, V_{BE} are assumed to be the same for $\Delta I_{B,for}$ and $\Delta I_{B,rev}$, then the ratio of forward- and inverse base current leakage can be found to be

$$\frac{\Delta I_{B,rev}}{\Delta I_{B,for}} = \frac{P_{E,rev} \sigma_{rev}}{P_{E,for} \sigma_{for}} \approx 1.5 \frac{\sigma_{rev}}{\sigma_{for}} \approx 5 \tag{2}$$

$P_{E,rev}$ and $P_{E,for}$ were calculated from the layout dimensions of the emitter opening and the bounds of the SIC implant. Therefore it can be seen that the forward-mode trap density is increasing at approximately 30% of the rate of inverse mode trap density during stress. This indicates that 30% of the hot carriers generated in the CB junction are able to travel towards the EB spacer and produce damage. This ratio in older SiGe generations was found to be about 10% for SiGe HBT B, and 1.7% for SiGe HBT C. Thus, it could be seen that the forward-mode is more easily damaged for scaled SiGe HBTs. For such

aggressively scaled devices, not only are hot carriers more energetic as a result of inherently higher electric fields, they are also more likely to travel through the base and cause damage in the EB-spacer, given their closer proximity. This is consistent with the current-sweep results shown in Figure 7. The 2nd generation SiGe HBT shows a smaller hump region compared that of the 3rd generation device, and for the 1st generation device, the damage is barely noticeable.

CHAPTER 5

REGION II: MIXED-MODE ANNEALING

Mixed-mode annealing occurs on the falling edge of the hump shaped damage response, and follows a logarithmic time-dependence, as shown in Figure 11. Two SiGe HBT A devices were first damaged in Region I and then subjected to mixed-mode annealing, and interestingly the low current induced damage can be removed with a subsequent higher $J_{E,str}$. Additional experiments demonstrated that reverse-EB stress could be recovered via mixed-mode annealing, which is can be seen in Figure 12 and Figure 13, where two configurations of reverse-EB stress were used: open-collector (OC), which is dominated by hot holes, and forward-collector (FC), which is dominated by hot electrons [15]. The forward-collector configuration damages devices substantially faster than the open-collector, which is due to the fact that large amount of electrons were injected into the EB junction. However, more than 90% of the damage was subsequently removed by mixed-mode annealing. In both configurations of reverse-EB stress, the ideality factor of $\Delta I_{B,for}$ is close to 1.8, again a classical SRH recombination mechanism.

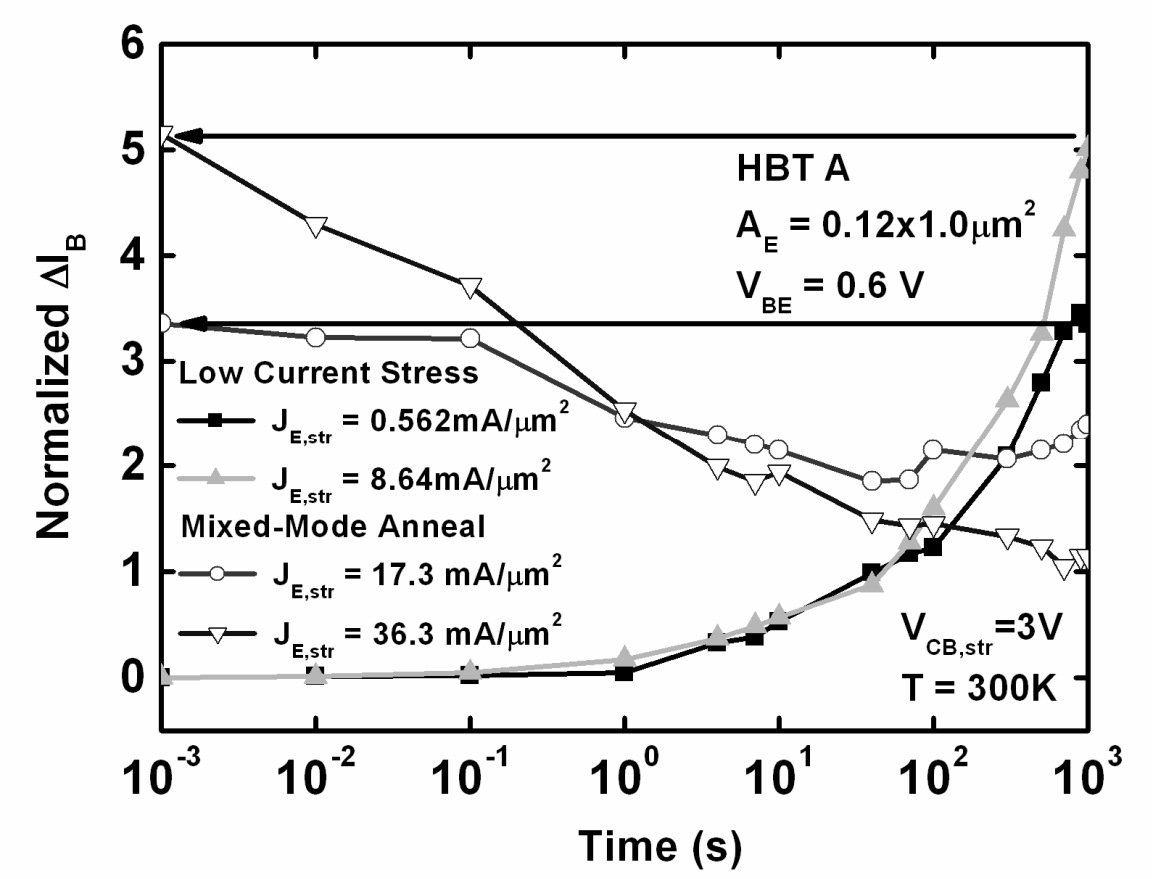

Figure 11. The mixed-mode annealing of HBT A's subjected to low-current damage. Low-current stress and mixed-mode annealing is observed to be a strong function of $J_{E,str}$. Normalized ΔI_B is defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

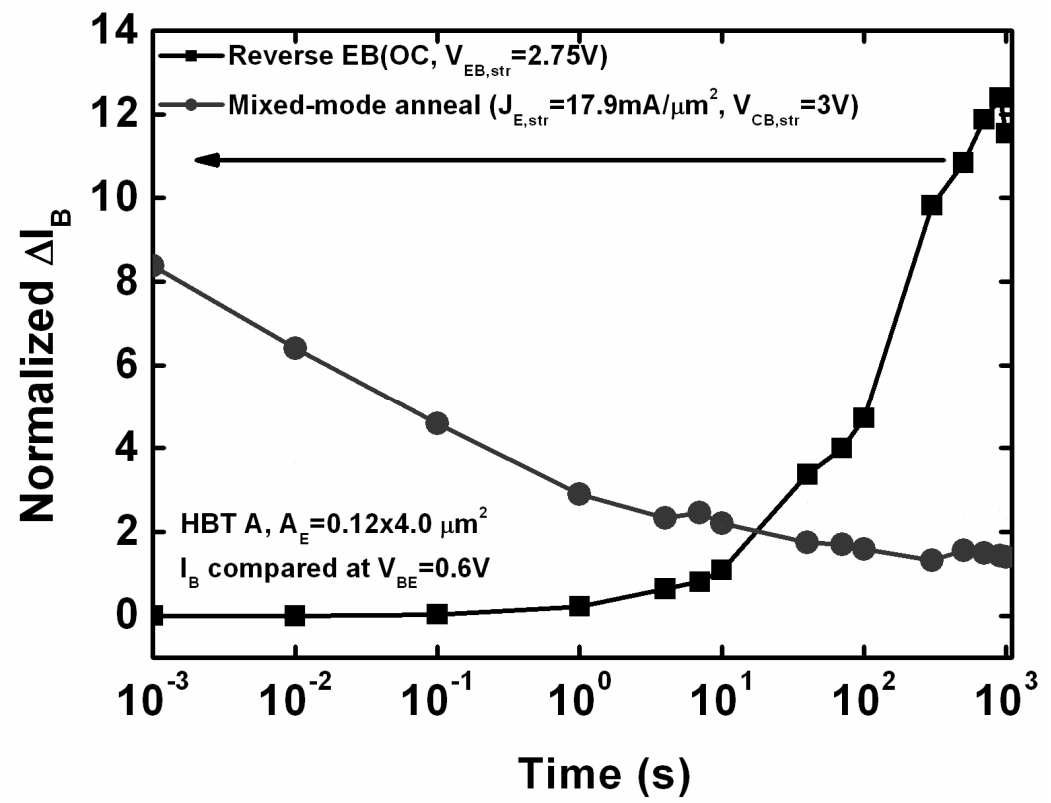

Figure 12. The mixed-mode annealing of Open-Collector reverse-EB stress of SiGe HBT A. Normalized ΔI_B was defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

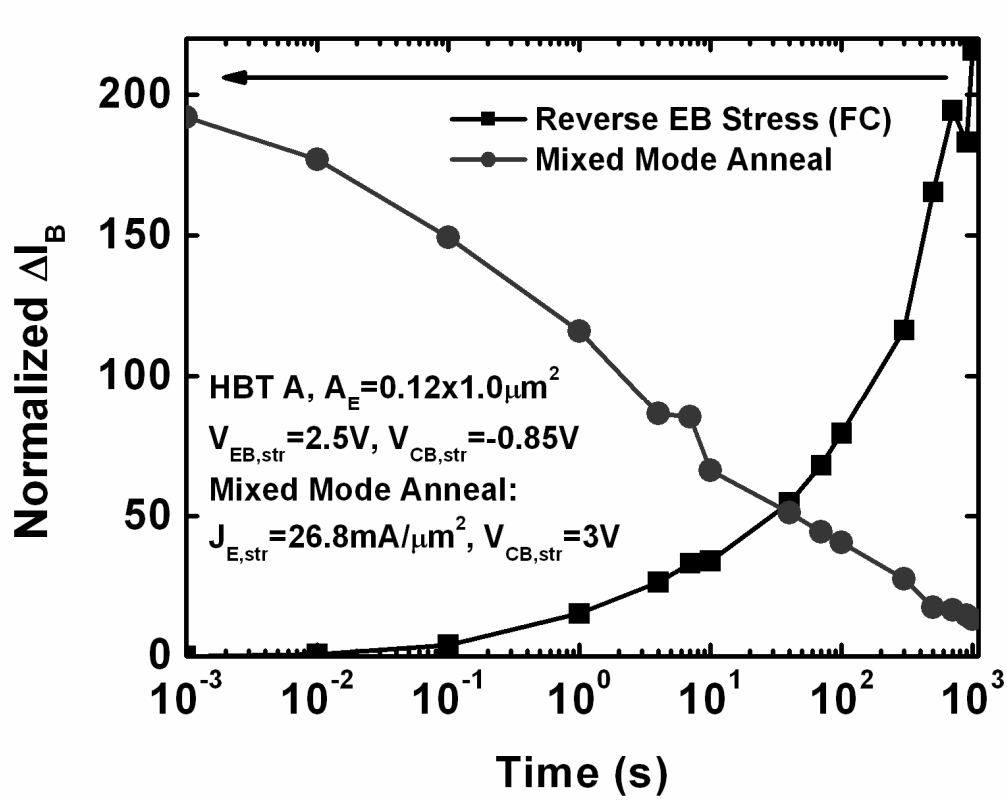

Figure 13. Stress-induced leakage current due to forward-collector mode reverse-EB stress, and subsequently its removal by mixed-mode annealing.

Thermal annealing experiments were performed on damaged devices. Devices were first stressed in Region I, and subsequently thermally-annealed in an inert ambient for 15 minutes. After post-anneal measurements, the devices were annealed at a higher temperature, etc. As shown in Figure 14, a large amount of $\Delta I_{B,for}$ can be removed at 200ºC. In addition, thermal annealing experiments of reverse-EB stressed devices have been reported, and it was found that reverse-EB leakage current could be also removed at 200ºC in an inert ambient [16].

The fact that base leakage due to both Region I stress and reverse-EB stress can be removed by either mixed-mode annealing or thermal annealing leads to two observations. First, given the similar ideality factor and annealing characteristics, Region I stress and reverse-EB stress produce the same type of interface trap, most probably a silicon dangling bond. Second, given that $\Delta I_{B.for}$ can be removed by temperature alone proves that mixed-mode annealing is essentially a self-heating phenomenon. Taking an SiGe HBT A with A_E=0.12x1.0 μm^2 and $J_{E,str}$=30 mA/μm^2 as an example, the junction temperature can be estimated as

$$T_j = P_{diss} R_{th} + T_{amb} = \left(I_C V_{CB} + I_C V_{BE} + I_B V_{BE}\right) R_{th} + T_{amb} \approx 204\,^{\circ}C \qquad (1)$$

This agrees well with the thermal annealing results.

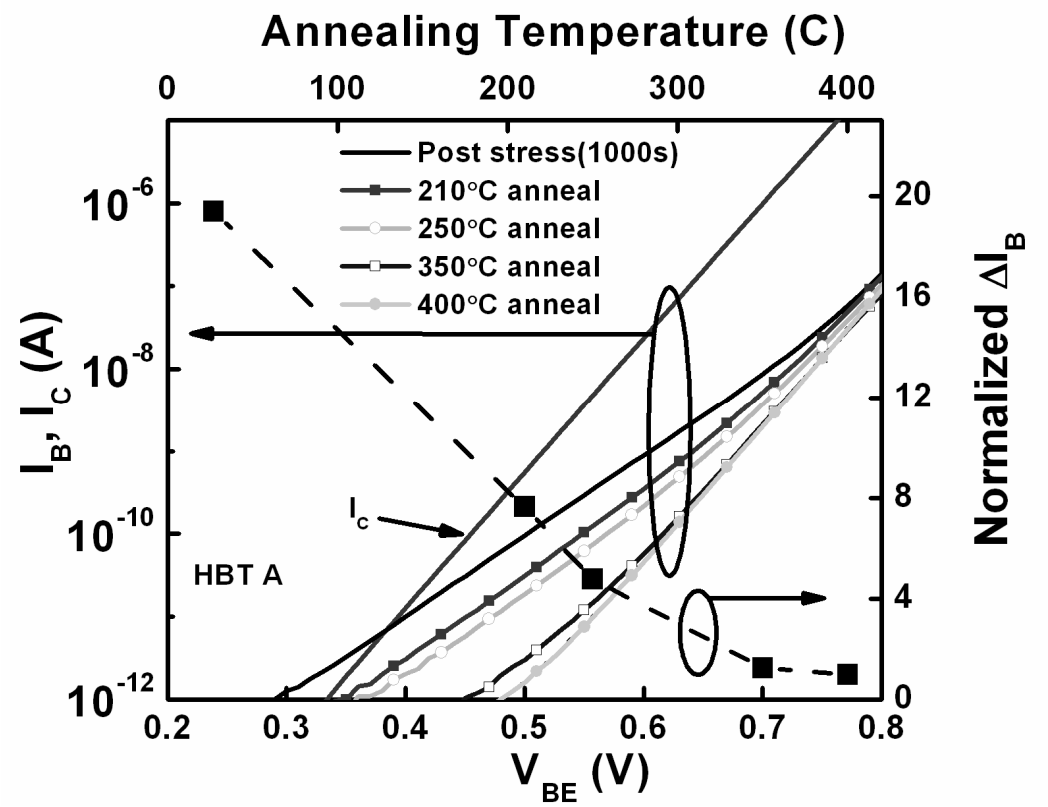

Figure 14. Base leakage current during thermal annealing. Devices were first low-current stressed, and then subjected to thermal annealing in an inert ambient for 15 minutes.

CHAPTER 6

REGION III: HIGH-CURRENT MIXED-MODE DAMAGE

The Region III high-current damage region refers to the rapid-rise region immediately to the right of the hump shape in the stress response. This region has different temperature, geometry, and annealing characteristics than that of Region I. Figure 15 plots the current sweeps of SiGe HBT A with A_E of 0.12x1.0 μm^2, 0.12x2.0 μm^2, 0.12x4.0 μm^2, and 0.12x8.0 μm^2, which shows that the high-current region occurs at different $J_{E,str}$; that is, the current density threshold ($J_{E,thres}$) at which damage was observed occurs sooner for larger devices. This is more clearly seen in the inset, where the current damage threshold is plotted as $I_{E,thres}$. The calculated junction temperatures at the damage thresholds appear to be the same, therefore it can be inferred that high-current damage requires a certain critical junction temperature to initiate interface damage. This is further supported by data in Figure 16, in which current-sweeps at different ambient temperatures are plotted, and with the reverse-mode data plotted in the inset. Higher ambient temperature implies that less self-heating is needed to reach the critical junction temperature for damage; therefore, less $J_{E,str}$ should be required to trigger the high-current damage. This critical junction temperature is seen across all investigated technologies. The temperature dependence is contrary to the classical hot carrier damage, because hot carrier damage normally decreases with increasing temperature due to enhanced scattering, and it does not require a critical temperature to activate.

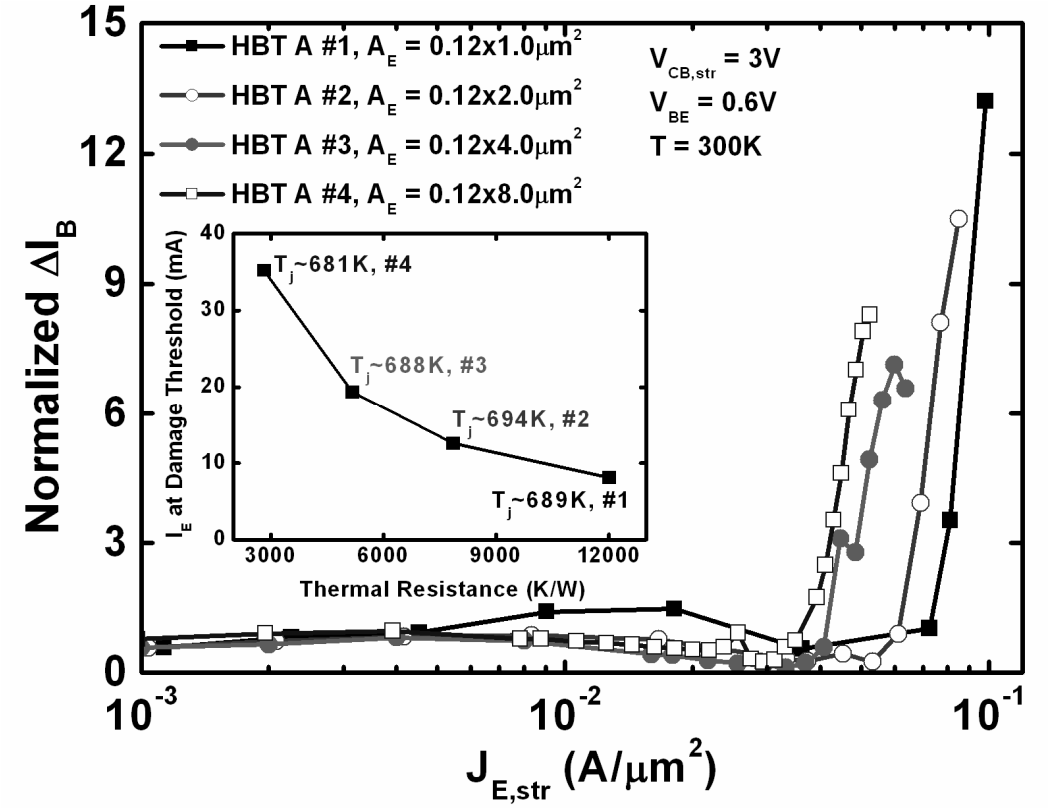

Figure 15. Stress current-sweeps of 4 SiGe HBTs with varying geometry. The inset plots the threshold at which high-current damage occurs. The junction temperature at which the damage occurs is about the same for these devices. Normalized ΔI_B is defined as $(I_{B,post}-I_{B,pre})/I_{B,pre}$.

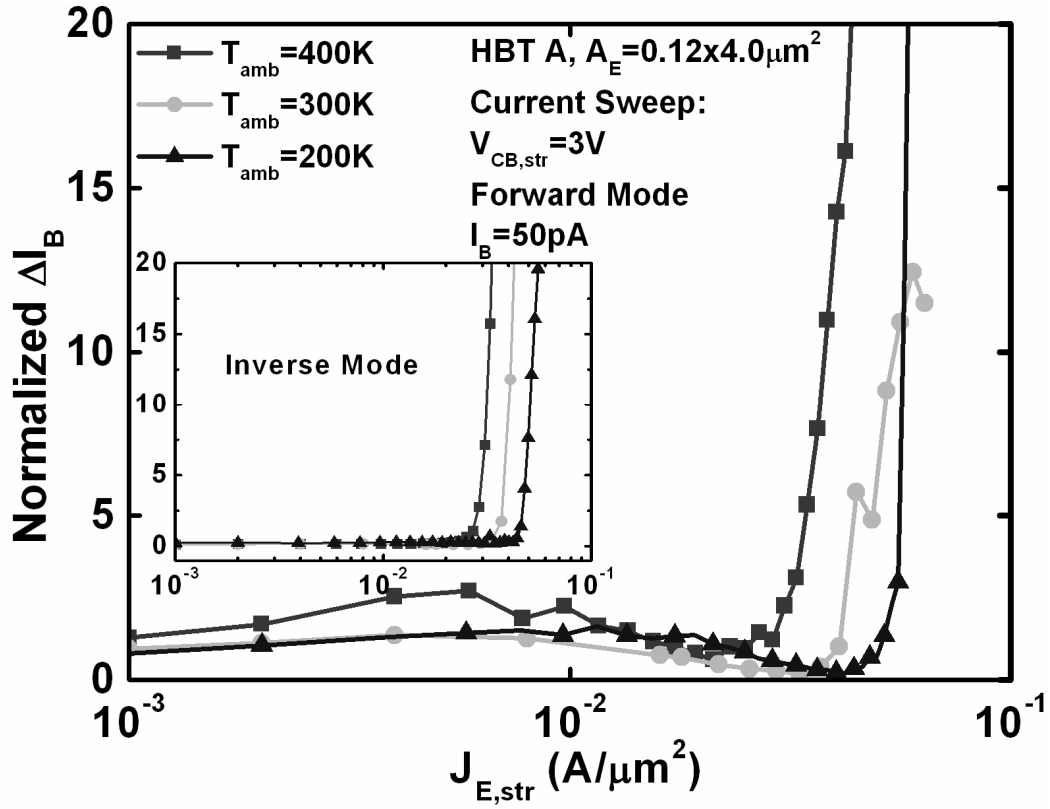

Figure 16. Current sweeps of SiGe HBT A at different ambient temperatures. Normalized ΔI_B was measured at I_B = 50 pA. The reverse mode damage is shown on inset. As temperature increases, the threshold of high-current damage appears sooner.

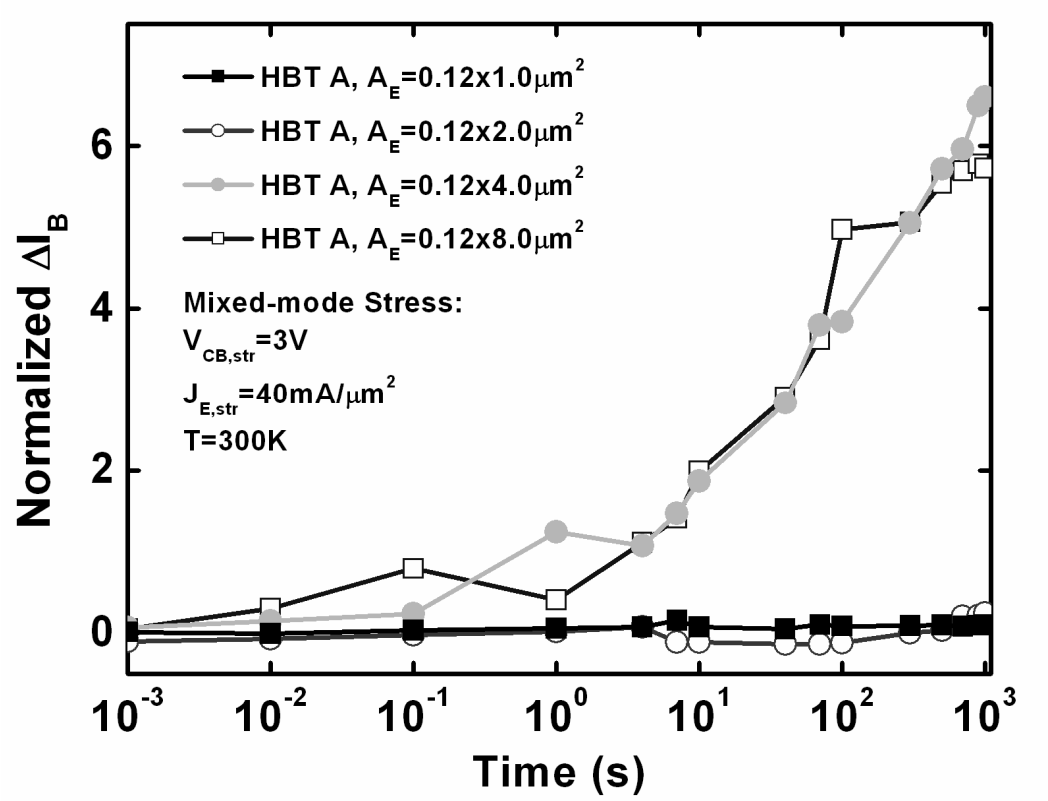

Figure 17. Time-dependent mixed-mode stress of SiGe HBT A's, with varying geometries with $J_{E,str}$ = 40 mA/μm^2. The two large devices suffer substantial base leakage, while the two large devices suffer negligible damage.

The existence of a critical $J_{E,str}$ is further confirmed in Figure 17, where SiGe HBT A of different A_E's were stressed with the same $J_{E,str}$, $V_{CB,str}$, stress time interval, and ambient temperature. The two smaller devices show negligible damage, whereas the two larger devices show considerable base leakage. This can be explained by noting that the stress current density is less than the $J_{E,thres}$ of the two smaller devices but greater than $J_{E,thres}$ of the two larger devices. Thus the two large devices were damaged while the two smaller devices were not.

The annealing characteristics of low- and high-current damage are also very different. Figure 18 shows the mixed-mode annealing experiment performed after high-current stress damage. The device was high-current stressed for 10 s, then followed by mixed-mode annealing for 1000 s. The device was then stressed with the same stress condition, until it reached total stress time of 100 s, and then mixed-mode annealed for the second time. The device was then stressed up to total of 1000 s, and was once again mixed-mode annealed. As shown by in Figure 18, mixed-mode anneal had no effect on high-current damage.

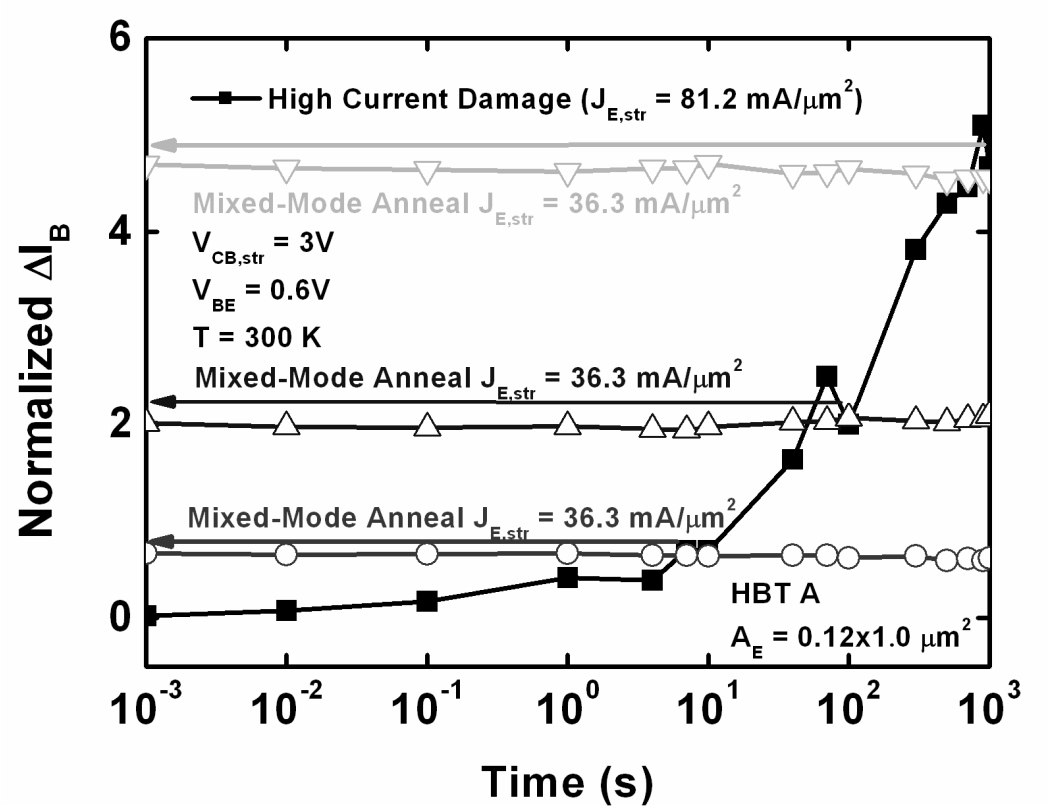

Figure 18. The mixed-mode annealing of high-current damage, in which the high-current damage was interrupted at 10, 100, and 1000 seconds to conduct mixed-mode annealing. The base leakage current remained constant with annealing, indicating damage was not annealed.

The interplay between mixed-mode annealing and high-current damage can be highly problematic for conducting mixed-mode stress experiments, since increasing emitter stress current is the typical way for accelerating stress [10, 17]. For example, it was reported that SiGe HBT B with geometry of 0.2 x 4.0 μm^2 did not suffer any damage up to $J_{E,str}$ of 20 $mA/\mu m^2$ and $V_{CB,str}$ of 3V [10]. The calculated junction temperature is estimated to be 542 K (294 ºC), which is well within the mixed-mode annealing region; the reason no damage was observed was because mixed-mode annealing was triggered. Then damage was observed when $J_{E,str}$ was increased to 35 $mA/\mu m^2$, however the estimated junction temperature in this case is around 743 K, and from Figure 15 it is clear that the device was being stressed in the high-current damage region. Thus, the damage mechanism can not be cleanly attributed to the classical hot carrier damage, as claimed in [10]. In addition, this implies that increasing $J_{E,str}$ above $J_{C,peak\ fT}$ to extract reliability lifetime is actually underestimating the damage, since increasing, $J_{E,str}$ would only be correct if the damage mechanism remains the same with $J_{E,str}$, which is generally not the case for mixed-mode stress.

CHAPTER 7

EXAMPLE: DAMAGE SPECTRUM OF SIGE HBT C

Having described the various damage responses for SiGe HBT A, it is now possible to quantify the complete damage spectrum. This is relevant for analyzing stress during circuit operations, since a wide range of circuit-relevant voltages and currents are possible. In addition, knowledge of the complete damage response is clearly important for reliability lifetime extraction, since errors in inferred lifetime would result if one unknowingly encroaches on the mixed-mode annealing region during accelerated stress.

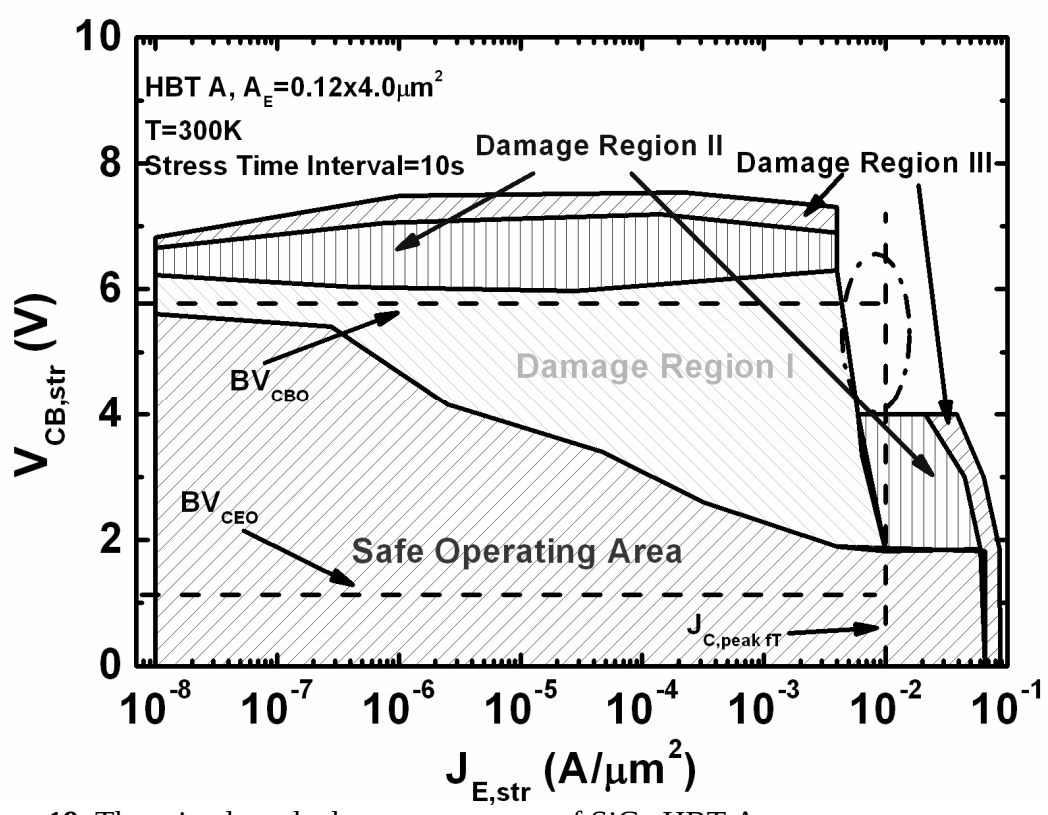

Figure 19. The mixed-mode damage spectrum of SiGe HBT A.

SiGe damage response during normal circuit-relevant biasing with addition to both off-state and extremely severe stress conditions were studied. The current-sweep was used due to its time efficiency; instead of maintaining constant $V_{CB,str}$ and increasing $J_{E,str}$, both parameters were increased. Each path taken by the current-sweep measurements can be viewed as radius of a circle with the origin at $V_{CB,str}$ = 0 V and $J_{E,str}$=10 nA/μm^2. Eight current sweeps are measured, and are spread out to cover $V_{CB,str}$ from 0 V to 8 V, and $J_{E,str}$ from 10 nA/μm^2 to 100 mA/μm^2. Using this method, a representative damage spectrum can be observed for a given device and technology of interest. Of course, as stress time intervals are increased, the damage spectrum is expected to change, and this should also be quantified.

Figure 19 illustrates the damage spectrum of SiGe HBT A, with A_E = 0.12x4.0 μm^2, at 300 K. The stress time interval was fixed at 10 seconds. The Safe Operating Area (SOA) here is defined as the region of I_B degradation less than 15%, at V_{BE}=0.6 V. The three damage regions are defined the same way as described in Section IV. For $J_{E,str}$ from 10 nA/μm^2 to 100 nA/μm^2, no damage is observed until $V_{CB,str}$ is around 5.6 V, near the BV_{CBO} of SiGe HBT A. However, when $V_{CB,str}$ is at and above BV_{CBO}, damage was actually reduced. This can be expected if the avalanche current due to junction breakdown becomes large enough to activate mixed-mode annealing. At even higher $V_{CB,str}$, the damage eventually increased again due to high-current damage. For $J_{E,str}$ from 100 nA/μm^2 to 7 mA/μm^2, the damage response remained the same, except that Region I occurs at a lower $V_{CB,str}$. The boundary between the Safe Operating Area and damage Region I is logarithmically related to $J_{E,str}$, while linearly related to $V_{CB,str}$. This agrees with previous stress studies [18], which finds that device lifetime is more dependent on $V_{CB,str}$ than $J_{E,str}$. For $J_{E,str}$ from 7 nA/μm^2 to 60 mA/μm^2, the device is in its Safe Operating Area from $V_{CB,str}$= 0 V to 1.8 V, and mixed-mode annealing occurs from 3 V to 4 V. At higher $V_{CB,str}$, the devices entered into a complicated combination of the three damage responses. In this region, mixed-mode annealing was expected to be activated;

however, damage was no longer fully removed. This was likely due to the high $V_{CB,str}$, which causes low-current damage to offset the annealing effect.

CHAPTER 9

SUMMARY AND FUTURE WORK

We have introduced an electrical stress methodology called “mixed-mode current-sweep”. Using this technique, three different damage regions have been identified: 1) low-current mixed-mode stress, 2) mixed-mode annealing, and 3) high-current mixed-mode stress. Stress region I, low-current mixed-mode stress, is associated with hot carriers created in the collector-base junction. With more aggressive scaling not only are more hot carriers created at the same stress condition, but also a larger percentage of the hot carriers generated in the CB junctions are able to travel to the EB spacer and create interface damage. This scaling-induced increase in stress damage poses a serious reliability concern. Stress region II, mixed-mode annealing, is a self-heating induced effect that can be seen under high stress conditions, and it is shown to have significant impact on accurately assessing reliability lifetime. Stress region III, high-current mixed-mode stress, occurs under extremely aggressive stress conditions, and has a very different damage response than for traditional hot carrier stressing. Finally, the overall damage spectrum of third-generation SiGe HBTs is presented in the context of three aforementioned damage regions.

More work is still needed in the field of SiGe reliability. The current work here only sheds light on the regions and interactions of various damage mechanisms; however it does not model the induced damage. Traditionally, devices are driven in “accelerated” stress conditions, such as at increased current density, in order to extract the reliability lifetime; stressing devices at normal operating conditions will simply take forever. By performing various accelerated stresses, one can then obtain the lifetime through extrapolation. However, as this work has shown, stress conditions must be very

methodically planned out, as to avoid the troubling regions such as mixed-mode annealing. Therefore the work presented here is very important to lifetime prediction.

That being said, the current work is still incomplete in assessing the device operating lifetime, and future work will be needed to address this. Using the various regions of damage as a guide (for example Figure 19), damage needs to be separately characterized: its dependence on stress time, emitter current, and collector voltage. With the existing trap generation models such as the reaction-diffusion model, hot carrier models such as the lucky-electron model, and using Shockley-Reed-Hall generation-recombination current, the mixed-mode damage can then be accurately modeled. Damage models are very important now in the field of high-frequency, mixed-signal systems, because the interactions due to different stages in the circuit and the degradation due to progressive scaling are *highly* unpredictable. If such model is made available then it can be transformed into a Verilog-A component, allowing the circuit designer to observe directly the device damage *and* how it affects the overall circuit/system.

APPENDIX A

SRH CALCULATION AND SIMULATION

In studies of bipolar reliability, the generation-recombination current due to traps presents the most fundamental damage characteristics. This current component was studied long time ago by the famous Shockley, Read and Hall, and their work is now commonly known to be the SRH g-r current.

Although SRH g-r current has been known for a long time, few know its subtleties and its effects on modern bipolar technologies such as SiGe HBTs. Particularly, the effect of trap energy has been confusing to some. It was argued by some that the ideality factor of the SRH g-r current is not dependent on the trap energy level; in other words having ideality factor of 2 does not indicate traps at the midgap. This appendix seeks to shed light on this subject, through Matlab calculations and T-Cad simulations.

In the simplified condition the SRH g-r current is described in Sze's Physics of Semiconductor Devices (2^{nd} edit. eq. 59, p. 37)

$$U = \sigma v_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)} \tag{3}$$

Sze's book states,

"The recombination rate approaches a maximum as the energy level of the recombination center approaches midgap (i.e. $E_t \sim E_i$)."

However, it is not that simple. Shown from the equation above, the *cosh* term is affected by the difference in trap energy level (E_t) and midgap (E_i), but its effect largely depends on values of *n* and *p*. The larger the *cosh* term becomes with respect to *n* and *p*, the smaller the recombination gets. Plotting eq (3) in Figure 20:

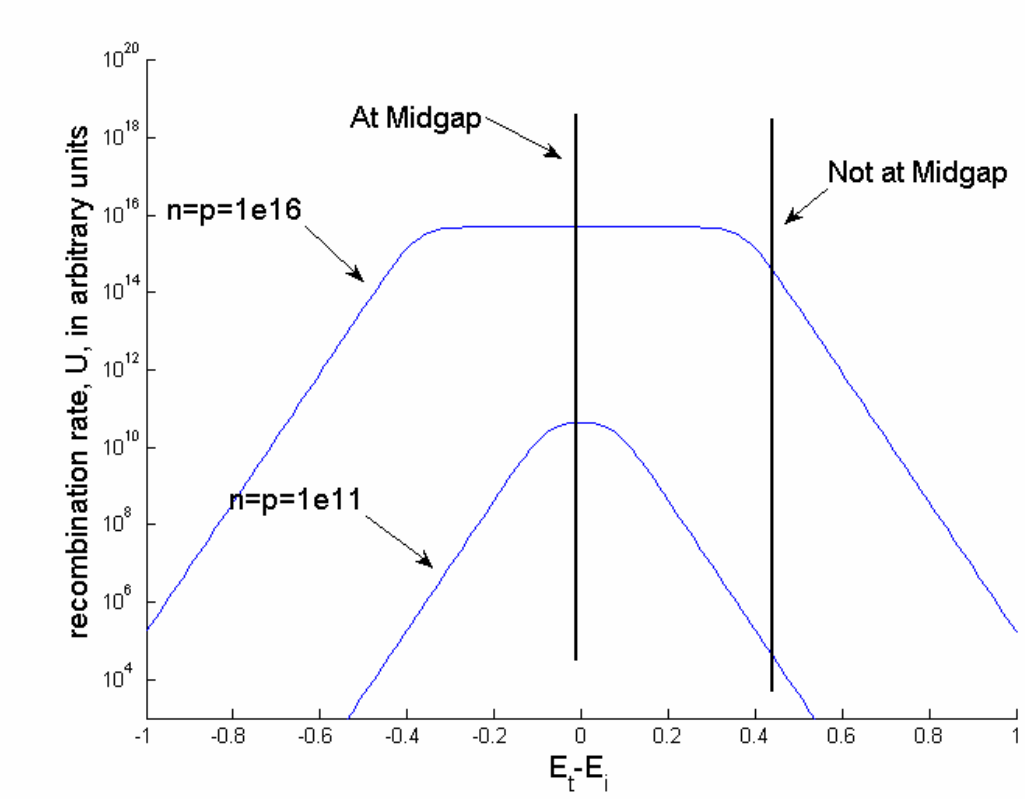

Figure 20. Recombination rate as function of trap energy.

At low injection the recombination is dominated by traps at midgap; the *cosh* term grows very large (because *n* and *p* are small) such that traps away from the midgap will not contribute to any g-r current. In other words, at low injection traps not at midgap will have lower recombination than traps at midgap. As current density increases, *n* and *p* becomes very large, such that the *cosh* term doesn't contribute at all, until 0.5 eV away from the midgap. This means that at high injection trap energies are irrelevant; traps at any level will give the same recombination rate.

In simplifying our analysis, let's suppose there is only one type of trap in the oxide with a fixed energy level. If the trap is at midgap, then *cosh* term falls away, and thus the only thing that affects the ideality factor would be the carrier concentrations in the pn junction. Since the carrier concentrations in a pn junction is characterized by solving for the minority carrier concentrations, the n and p each naturally carries an $e^{qV/kT}$ term, which combines to make the classical *2kT* slope (this will be made clearer in later sections). If the trap is not at midgap, then there will be an additional *cosh* term contributing to the slope: as seen from the "Not at Midgap" line in Figure 20, at low injection it is far away from the peak recombination rate due to the *cosh* term. This means that g-r current would be very small in low injection. Yet at higher injection it is very close to peak recombination rate, since *cosh* term becomes much less significant. Given this observation we can predict that when traps are not at midgap the ideality factor would be less (high ideality factor implies slow-rising slope, low ideality factor implies strong-rising slope) at low injection than it is at higher injection.

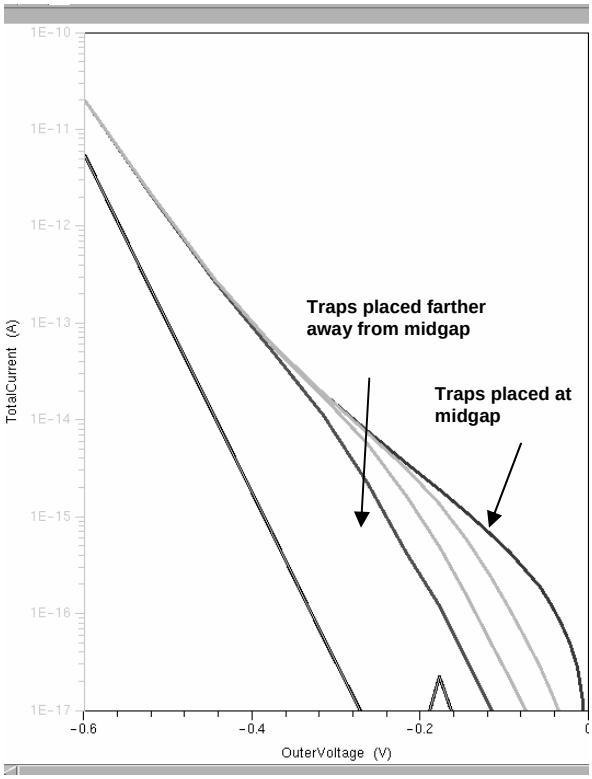

Figure 21. T-CAD simulation of the SRH g-r current, with varying trap energy levels.

Figure 21 shows device simulations in Dessis of SiGe HBT A. The lowest line indicates base current without SRH g-r current. With traps created at midgap, the leakage current exhibits a ~*2kT* slope, as expected. As traps energy is moved farther away from the midgap, we can observe that the g-r current is less at low injection (e.g., $V_{BE} < 0.15$ V), but overlay with the midgap traps at higher injection. The farther the traps are placed from midgap, the less it is at low injection. The expected low ideality factor in low injection can be also observed.

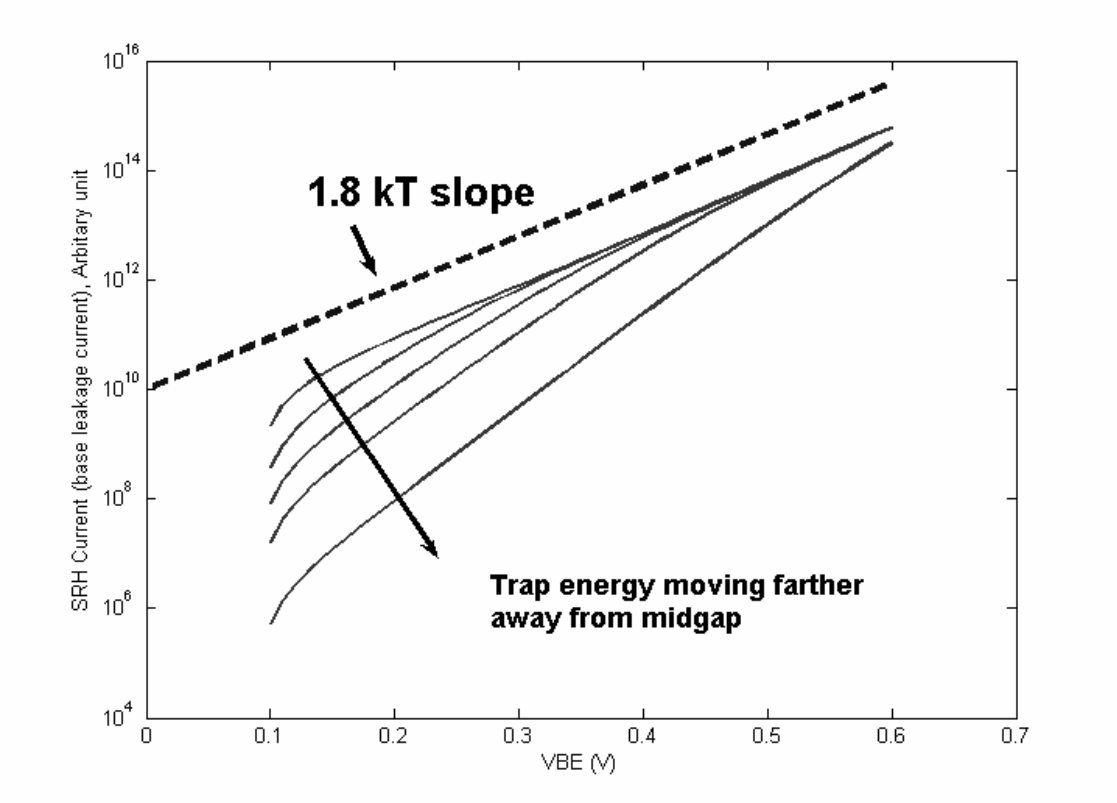

Figure 22. Matlab simulation of the SRH g-r current.

The effect of the trap energy level is further studied by Matlab simulation of a leakage current in an ideal and symmetric pn junction, shown in Figure 22. The simplified SRH equation mentioned previously is used to calculate this. The same characteristics are observed; with traps at midgap leakage current has ideality factor around 2. As traps are placed farther away from midgap, then at high enough injection the ideality factor can recover back to ~2.

Figure 22 shows that for the midgap traps, at ideality factor of 1.8 was calculated. This is slightly less than the 2 that is normally expected, and this has to do with the spacial locations of the trap. Again we use the SRH g-r equation mentioned earlier; assuming traps are in midgap (so the *cosh* term falls away). At high enough injection the n_i^2 term can be neglected, and the equation can be further simplified to

$$U \approx \sigma v_{th} N_t \frac{pn}{n+p} \tag{4}$$

Now inside the pn depletion the carriers at a location *x* can be calculated to be

$$n(x) \approx N_D e^{-\frac{q}{kT}\cdot\frac{x}{W}\cdot(Vbi-Vbe)} \tag{5}$$

and

$$p(x) \approx N_A e^{-\frac{q}{kT}\cdot(1-\frac{x}{w})\cdot(Vbi-Vbe)} \tag{6}$$

Where the n-type semiconductor is at $x < 0$, from $0 < x < w$ is the pn depletion the p-type semiconductor is at $x > w$. At the middle of the depletion region ($x = w/2$) and assuming a symmetric junction ($N_A = N_D$), U can be further simplified to be

$$U \approx \sigma v_{th} N_t \frac{pn}{n+p} = \sigma v_{th} N_t n \propto e^{\frac{qVbe}{2kT}} \tag{7}$$

This gives the classical $2kT$ slope. But close to the p-side (x near w) $N_A \sim p >> n \sim N_D * e^{-q(Vbi-Vbe)/kT}$, and close to the n-side (x near 0) $N_D \sim n >> p \sim N_D * e^{-q(Vbi-Vbe)/kT}$, then U becomes

$$U \approx \sigma v_{th} N_t \frac{pn}{n+p} = \sigma v_{th} N_t n \propto e^{\frac{qVbe}{kT}} \tag{8}$$

Or

$$U \approx \sigma v_{th} N_t \frac{pn}{n+p} = \sigma v_{th} N_t p \propto e^{\frac{qVbe}{kT}} \tag{9}$$

Which means that recombination far away from the middle of the pn junction (where $p = n$) would actually give a $1kT$ slope. Thus, the *total* SRH g-r current will not quite be $2kT$, but $\sim 1.8\ kT$. Interestingly, this is consistently observed in stress measurements shown in previous sections; the mean of the ideality factor is $1.8\ kT$, fitting the SRH theory very well.

REFERENCES

[1] G. Zhang, J. D. Cressler, G. Niu, and A. J. Joseph, "A new "mixed-mode" reliability degradation mechanism in advanced Si and SiGe bipolar transistors," *IEEE Transactions on Electron Devices,* vol. 49, pp. 2151-6, 2002.

[2] A. Appaswamy, M. Bellini, W.-M. L. Kuo, P. Cheng, J. Yuan, C. Zhu, J.D. Cressler, G. Niu, and A. Joseph, "Impact of Scaling on the Inverse Mode Operation of SiGe HBTs," *IEEE Transactions on Electron Devices,* in press.

[3] P. Cheng, C. Zhu, J.D. Cressler, and A. Joseph, "A New Current Sweep Method for Assessing the Mixed-Mode Damage Spectrum of SiGe HBTs" *IEEE Transactions on Device Materials and Reliability*, 2007, in press.

[4] B. Jagannathan, M. Khater, F. Pagette, J. S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, S. J. Jeng, J. Johnson, E. Mengistu, K. T. Schonenberg, C. M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Letters,* vol. 23, pp. 258-260, 2002.

[5] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, P. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Meghelli, and A. Rylyakov, "A 0.18 □m BiCMOS technology featuring 120/100 GHz (f_T/f_{max}) HBT and ASIC-compatible CMOS using copper interconnect," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2001, pp. 143-146.

[6] D. L. Harame, D. C. Ahlgren, D. D. Coolbaugh, J. S. Dunn, G. G. Freeman, J. D. Gillis, R. A. Groves, G. N. Hendersen, R. A. Johnson, A. J. Joseph, S. Subbanna, A. M. Victor, K. M. Watson, C. S. Webster, and P. J. Zampardi, "Current status and future trends of SiGe BiCMOS technology," *IEEE Transactions on Electron Devices,* vol. 48, pp. 2575-2594, 2001.

[7] M. Racanelli and P. Kempf, "SiGe BiCMOS technology for communication products," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2003, pp. 331-334.

[8] T. Vanhoucke, H. M. J. Boots, and W. D. van Noort, "Revised method for extraction of the thermal resistance applied to bulk and SOI SiGe HBTs," *IEEE Electron Device Letters,* vol. 25, pp. 150-152, 2004.

[9] J. S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman, and S. Subbanna, "Measurement and modeling of thermal resistance of high speed SiGe heterojunction bipolar transistors," *Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems,* 2001, pp. 110-113.

[10] C. Zhu, Q. Liang, R. A. Al-Huq, J. D. Cressler, Y. Lu, T. Chen, A. J. Joseph, and G. Niu, "Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of SiGe HBTs," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 142-9, 2005.

[11] G. Freeman, J.S. Rieh, B. Jagannathan, Y. Zhijian, F. Guarin, A. Joseph, and D. Ahlgren, "SiGe HBT performance and reliability trends through f_T of 350 GHz," in *Proceedings of IEEE International Reliability Physics Symposium,* Dallas, TX, USA, 2003, pp. 332-338.

[12] T. M. Liu, T. Y. Chiu, V. D. Archer, III, and H. H. Kim, "Characteristics of impact-ionization current in the advanced self-aligned polysilicon-emitter bipolar transistor," *IEEE Transactions on Electron Devices,* vol. 38, pp. 1845-1851, 1991.

[13] T. Vanhoucke, G. A. M. Hurkx, D. Panko, R. Campos, A. Piontek, P. Palestri, and L. Selmi, "Physical Description of the Mixed-Mode Degradation Mechanism for High Performance Bipolar Transistors," *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting,* 2006, pp. 1-4.

[14] S. L. Kosier, A. Wei, R. D. Schrimpf, D. M. Fleetwood, M. D. DeLaus, R. L. Pease, and W. E. Combs, "Physically based comparison of hot-carrier-induced and ionizing-radiation-induced degradation in BJTs," *IEEE Transactions on Electron Devices,* vol. 42, pp. 436-444, 1995.

[15] U. Gogineni, J. D. Cressler, G. Niu, and D. L. Harame, "Hot electron and hot hole degradation of UHV/CVD SiGe HBT's," *IEEE Transactions on Electron Devices,* vol. 47, pp. 1440-1448, 2000.

[16] S. R. Sheng, S. P. McAlister, J. P. McCaffrey, and S. J. Kovacic, "Degradation and recovery of SiGe HBTs following radiation and hot-carrier stressing," *Solid-State Electronics,* vol. 48, pp. 1901-1906, 2004.

[17] A. Piontek, T. Vanhoucke, S. Van Huylenbroeck, L. J. Choi, G. A. M. Hurkx, E. Hijzen, and S. Decoutere, "The influence of lateral device scaling and airgap deep trench isolation on the reliability performance of 200 GHz SiGe:C HBTs," *Semiconductor Science and Technology,* vol. 22, pp. 9-12, 2007.

[18] D. Panko, T. Vanhoucke, R. Campos, and G. A. M. Hurkx, "Time-to-fail extraction model for the "mixed-mode" reliability of high-performance SiGe bipolar transistors," in *Proceedings of IEEE International Reliability Physics Symposium*, 2006, pp. 512-515.